

L42 ANSWER 15 OF 29 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
 AN 1998-156322 [14] WPIX
 DNN N99-124947 DNC C1998-050336
 TI CMOS device - has gate insulating film formed over substrate,
 over which **germanium electrode layer** is
 formed.
 DC L03 U11 U13
 PA (SONY) SONY CORP
 CYC 1
 PI JP 10027854 A 19980127 (199814)* 6p H01L021-8238
 ADT JP 10027854 A JP 1996-180919 19960710
 PRAI JP 1996-180919 19960710
 IC ICM H01L021-8238
 ICS H01L021-336; H01L027-092; H01L029-78
 AB 10027854 A UPAB: 19980410
 The device has a semiconductor substrate on which a gate
 insulating film (23) is formed. A **germanium**
electrode layer (31) is formed on the gate insulating
 layer.
 ADVANTAGE - Enables production of surface channel type PMOS and NMOS
 using single polar gate electrode.
 Dwg 1/6
 FS CPI EPI
 FA AB; GI
 MC CPI: L04-C11C
 EPI: U11-C05F1; U13-D02A

6/9/9 (Item 9 from file 350)
 DIALOG(R) File 350 Derwent WPIX
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010404683 **Image available**

WPI Acc No: 1995-305997/199540

XRAM Acc No: C95-136432

XRPX Acc No: N95-232143

Semiconductor device e.g. MOST for LSI circuit - has double layered structure of gate electrode, consisting of polycrystalline silicon® film and germanium® film, formed over gate insulating film

Patent Assignee: TOSHIBA KK (TOKK)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicant No	Kind	Date	Week
JP 7202178	A	19950804	JP 93351053	A	19931228	199540 B

Priority Applications (No Type Date): JP 93351053 A 19931228

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 7202178	A	12	H01L-029/78	

Abstract (Basic): JP 7202178 A

The semiconductor device has a silicon substrate (11) on which a gate insulating film (12) is formed. The thickness of the insulating film is about 70nm thickness. A polycrystalline silicon film (13a) of 50nm thickness is formed over the insulating film by chemical deposition method. A polycrystalline germanium film (13b) of 0.3 micrometer thickness is grown externally on the low voltage chemical deposition method. This germanium film is formed over the silicon film and forms a gate electrode (13) by plasma etching.

ADVANTAGE - Ensures less power. Reduces impurity density of substrate sustains predetermined threshold voltage.

Dwg. 1/12

Title Terms: SEMICONDUCTOR; DEVICE; LSI; CIRCUIT; DOUBLE; LAYER; STRUCTURE;

L42 ANSWER 21 OF 29 WPIX COPYRIGHT 2003 THOMSON DERWENT ON STN
 AN 1991-122886 [41] WPIX
 CR 1992-131697 [16]

DNC C1993-145153

TI Deposition of germanium thin films on silicon dioxide - using interposed thin film of polycrystalline silicon as support in the fabrication of self-aligned MOS structures.

DC L01

IN OZTURK, M; WORTMAN, J
 PA (UVMC-N) UNIV NORTH CAROLINA STATE

CYC 1

PI US 5250452 A 19931005 (199341)* 7p H01L021-441

ADT US 5250452 A Div ex US 1990-515595 19900427, US 1991-717631 19910619

FDT US 5250452 A Div ex US 5101247

PRAI US 1990-515595 19900427; US 1991-717631 19910619

IC 1CM H01L021-441

AB US 5250452 A UPAB 19931130

Depositing polycrystalline Ge films on SiO₂ comprises: depositing a layer of polycrystalline Si on a SiO₂ layer, thick enough to support the deposition of polycrystalline Ge on it, while thin enough to be deposited sufficiently rapidly to substantially avoid deleterious effects on the characteristics of the oxide structure during the deposition process; exposing the polycrystalline Si layer to a Ge-contg. gas at a temp. below that at which Ge will deposit on SiO₂ alone while preventing native growth of SiO₂ on the polycrystalline Si layer, and for a time sufficient to deposit a layer of polycrystalline Ge upon the polycrystalline Si that is thick enough to mask the polycrystalline Si layer and underlying SiO₂ layer from ion implantation.

USE/ADVANTAGE - Method of using Ge thin films in combination with SiO₂ in the fabrication of self-aligned MOS structures, with the advantage of working with a low thermal budget.

Dwg.1,2/3
 FS CPI

L121 ANSWER 4 OF 8 HCAPLUS COPYRIGHT 2003 ACS on STN

AN 2000;600624 HCAPLUS

DN 1312;201733

TI Fabrication of semiconductor devices provided with depletion-decreased gate electrodes in MIS FETs

IN Mokami, Toru

PA Nec Corp., Japan

SO Jpn. Kokai Tokkyo Koho, 10 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

IC ICM HO1L021-8238

ICS HO1L027-092; HO1L029-43; HO1L029-78

CC 76-3 (Electric Phenomena)

PAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2000236028	A2	20000829	JP 1999-37200	19990216
JP 3261697	B2	20020304		

PRAI JP 1999-37200 19990216

AB The title fabrication involves (1) forming a **gate insulator film** on a component-isolated semiconductor substrate, (2) depositing a semiconductor film in doping a 1st cond.-type dopant according to the cond. for gate electrode as a 1st electrode formed on the **gate insulator film**, (3) depositing a conductor film without doping in formation of a gate electrode as a 2nd electrode film over the 1st electrode film, (4) doping a 2nd cond.-type dopant in prepn. of a 2nd cond.-type gate electrodes in the semiconductor device, (5) etching to pattern the 1st and 2nd gate electrodes, and (6) doping in prepn. of source/drain regions in the semiconductor devices. The process provides the semiconductor devices with depletion-decreased gate electrodes in MIS FETs.

IT 7440-56-4P Polysilicon, properties 7440-56-4P.

Germanium, properties

RL: DEV (Device component use); PNU (Preparation, unclassified); PRP (Properties); PREP (Preparation); USES (Uses)
 (gate electrode; fabrication of semiconductor devices provided with depletion-decreased gate electrodes in MIS FETs)

IT 7440-56-4P Germanium, properties

RL: DEV (Device component use); PNU (Preparation, unclassified); PRP (Properties); PREP (Preparation); USES (Uses)
 (gate electrode; fabrication of semiconductor devices provided with depletion-decreased gate electrodes in MIS FETs)

RN 7440-56-4 HCAPLUS

CN Germanium (7CI, 8CI, 9CI) (CA INDEX NAME)

Ge

JP priority 2/16/99
 JP pub date 8/29/00

L57 ANSWER 1 OF 1 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
 AN 2000-590915 [56] WP1X
 DNN N2000-437439 DNC C2000-176756
 TI Semiconductor device manufacturing method involves doping predetermined
 impurities on gate electrode areas of different polarities.
 DC L03 U11 U12
 PA (NIDE) NEC CORP
 CYC 1
 PI JP 2000236028 A 20000829 (200056)* 10p H01L021-8238
 ADT JP 2000236028 A JP 1999-37200 19990216
 PRAI JP 1999-37200 19990216
 IC ICM H01L021-8238
 ICS H01L027-092; H01L029-43; H01L029-78
 AB JP2000236028 A UPAB: 20001106
 NOVELTY - A gate insulating film is formed on the silicon substrate (10).
 The doping of predetermined impurities is performed to the gate electrode
 (61,62) areas of different electric polarities, which is provided on the
 respective electrode formation films.
 USE - For manufacturing of semiconductor device such as MIS type
 field effect transistor.
 ADVANTAGE - The impurity is doped during film formation and doping is
 performed at high concentration. The degradation of transistor capability
 is reduced.
 DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of
 semiconductor device manufacturing method.
 Silicon substrate 10
 Gate electrodes 61,62
 Dwg.1/6
 FS CPI EPI

L24 ANSWER 15 OF 21 CAPLUS COPYRIGHT 2003 ACS on STN

AN 1999:162136 CAPLUS

DN 130:176398

TI Germanium cold cathode electron sources and fabrication thereof

IN Kobayashi, Takeshi

PA Shinko Electric Industries Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 5 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

IC ICM H01J001-30

ICS H01J009-02; H01L029-66

CC 76-12 (Electric Phenomena)

Section cross-reference(s): 56

FAN.CNT

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 11067059	A2	19990309	JP 1997-222253	19970819

PRAI JP 1997-222253 19970819

AB The title cold cathodes comprise a Ge emitter electrode and a Ge gate electrode in adjacent positions each other formed over an insulator layer on a substrate, wherein an Al film is provided between the Ge electrode layers and the insulator layer so as to make Al diffused into the Ge electrode in forming an Al-doped Ge p-semiconductor by annealing. The Al-doped Ge p-semiconductor gives the cold cathodes better electron emission efficiency and increased lifetime.

IT 7440-56-4P, Germanium properties

RL: Doped source component; PEP (Physical, engineering or chemical processes); PNU (Preparation, unclassified); PRP (Properties); PREP (Preparation); PROC (Process); USES (Uses);
(Al-doped, p-semiconductor cold cathode; germanium cold cathode electron sources and fabrication thereof)

RN 7440-56-4 CAPLUS

CN Germanium (7CI, 8CI, 9CI) (CA INDEX NAME)

Ge

IT 7429-90-5, Aluminum, uses

RL: MOA (Modifier or additive use); USES (Uses)
(dopant, for annealing; germanium cold cathode electron sources and fabrication thereof)

RN 7429-90-5 CAPLUS

Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

L24 ANSWER 16 OF 21 CAPLUS COPYRIGHT 2003 ACS on STN
 AN 1996:64498# CAPLUS
 DN 125:343262
 TI Controlled grain size and location of Ge thin films on silicon dioxide by low temperature selective solid phase crystallization
 AU Vining, C. M.; Atwater, Harry A.
 CS Thomas J. Watson Lab. Applied Physics, California Inst. Technol., Pasadena, CA, 91125, USA
 SO Materials Research Society Symposium Proceedings (1996), 403(Polyocrystalline Thin Films: Structure, Texture, Properties, and Applications II), 113-118
 CODEN: MRSPPD; ISSN: 0272-9172
 PB Material Research Society
 DT Journal
 LA English
 CC 75-1 (Crystallography and Liquid Crystals)
 AB Selective solid phase crystal formation of grain size and location in polycryst. thin Ge films on amorphous SiO₂ substrates is described. The approach consists of selective solid phase crystallization via an alloy reaction at predefined nucleation sites, which consist of metal islands deposited on top of the amorphous Ge film, followed by lateral solid phase epitaxial growth. Grain sizes as large as 30 μm were achieved in 50 nm thick Ge films at <475 degree... B and P doping resulted in significant lateral solid-phase epitaxial growth rate enhancements.
 IT 7440-56-4. Germanium, processes
 RL: PEP (Physical, engineering or chemical process); PROC (Process) (controlled grain size and location of Ge thin films on silicon dioxide by low temp. selective solid phase crystn.)
 RN 7440-56-4 CAPLUS
 CN Germanium (7CI, 8CI, 9CI) (CA INDEX NAME)

Ge

IT 7440-42-8. Boron, processes
 RL: MOA (Modifier or additive use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses) (solid-phase epitaxy of boron-doped germanium on silica)
 RN 7440-42-8 CAPLUS
 CN Boron (8CI, 9CI) (CA INDEX NAME)

B

L103 ANSWER 15 OF 24 HCAPLUS COPYRIGHT 2003 ACS on STN

AN 1995-808348 HCAPLUS

DN 123-244385

TI Semiconductor device having germanium-silicon mixed crystal source-drain regions and its manufacture

IN Ando, Takeshi

PA Nippon Electric Co, Japan

SO Jpn. Kokai Tokkyo Koho, 5 pp.

CODEN: JKXKAF

DT Patent

LA Japanese

IC ICM HO1L029-78

CC 76-3 (Electric Phenomena)

PAN. CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 07169958	A2	19950704	JP 1993-317009	19931216
PRAI JP 1993-317009				19931216

AB The device has a Si substrate where a x-type (x = elec. cond. type) 1st surface region successively coated with a gate-insulating film and a gate electrode is sandwiched with a 2nd and a 3rd surface regions resp. coated with y-type (x . noteq. y) source and drain regions consisting of Ge or Ge-Si mixed crystal semiconductor layers. The title manuf. involves growth of the semiconductor layer on the 2nd and the 3rd regions on the substrate by selected CVD, followed by implantation of y-type dopants to form the source and drain regions. The method is useful for manuf. of CMOS and gave transistors with shallow junction.

IT 7631-86-9. Silicon oxide, processes
 RL DEV (Device component use); FEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
 (gate-insulating film; manuf. of semiconductor device having germanium-silicon mixed crystal source-drain regions)

IT 7440-21-3. Silicon, processes 7440-56-4. Germanium,
 processes 11148-21-3
 RL: DEV (Device component use); FEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
 (manuf. of semiconductor device having germanium-silicon mixed crystal source-drain regions)

L55 ANSWER 1 OF 1 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
 AN 1995-267403 (35) WPIX
 DNN N1995-205406 DNC C1995-121530
 TI Structure of MOSFET - provides source and drain domains of N type conductivity on second and third surface domains of P type conductivity.

DC L03 U12

PA (NIDEC) NEC CORP

CYC 1 PI JP 07169958 A 19950704 (199535)* 5p H01L029-78 <--

ADT JP 07169958 A UP 1993-317009 19931216

PRAI JP 1993-317009 19931216

IC JPM H01L029-78

AB JP 07169958 A UPAB: 19950905
 The MOSFET consists of a first surface domain (31) between a second surface domain (32) and a third surface domain (33) at surface of P type Si surface (1). A gate electrode (3) is provided through gate oxide film (2) on the first surface domain of P type conductivity.

A silicon oxide film (4) covers the whole gate electrode thereby creating side walls (5). The source and drain domains (10) are formed on the second and third surface domains of P type conductivity. The source and drain domains are composed of N type silicon layer (6) and N type germanium layer (7).

ADVANTAGE - Provides shallow junction with sufficient control.

Dwg.1/5
 FS CPI EPI

L103 ANSWER 21 OF 24 HCAPLUS COPYRIGHT 2003 ACS on STN

AM 1986-617398 HCAPLUS

DN 1986-617398

TI Complementary field-effect transistors

IN Mori, Kazutaka; Murata, Jun

PA Hitachi, Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 4 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

IC ICM H01L027-08

ICS H01L021-20; H01L029-78

CC 76-3 (Electric Phenomena)

Section cross-reference(s): 75

FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 6112364	A2	19860530	JP 1984-233106	19841107

FRAI JP 1984-233106 19841107

AB In a complementary MIS FET having n and a p-type MIS

FETs in which a gate insulator and a gate electrode are formed on p- and n-type regions, resp., p-Si and n-Ge are used for the p- and n-type regions, resp. Thus, after a p-type well region with n-type source and drain regions was formed in an n-Si substrate, n-Ge was epitaxially grown close to the p-type well region, and p+-type source and drain regions were formed in the n-Ge by diffusion of Ga or In. A MOS FET produced had equal channel conductances with a high hole mobility and no latch-up.

IT 7440-56-4, properties

RL: FRP (Properties)
(epitaxy of, in complementary MIS FET manuf.)

RN 7440-56-4 HCAPLUS

CN Germanium (7CI, 8CI, 9CI) (CA INDEX NAME)

Ge

IT 7440-74-6, uses and miscellaneous

RL: USES (Uses)
(source-drain region formation in germanium doped with, in complementary FET manuf.)

RN 7440-74-6 HCAPLUS

CN Indium (8CI, 9CI) (CA INDEX NAME)

In

L106 ANSWER 13 OF 13 HCAPLUS COPYRIGHT 2003 ACS on STN

AN 1982-1113359 HCAPLUS

DN 100-113359

TI This film MOSFET

PA Toshiba Corp., Japan

SO Jpn; Kokai Tokkyo Koho, 4 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

IC H01L021-84; H01L021-324; H01L029-78

CC 76-3 (Electric Phenomena)

FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 58186950	A2	1983/11/01	JP 1982-68845	1982/04/26
JP 030133149	B4	1991/11/20		

PRAI JP 1982-68845

1982/04/26

AB This film MOSFETs with good threshold voltages and mobilities of approx. 20 cm²/V-s are fabricated by depositing a film (e.g., Ge) with a large IR absorption on glass, depositing amorphous or polycryst. Si, masking with SiO₂, exposing to IR radiation to crystallize the film, implanting P ions in the source and drain regions, and forming the contacts.

IT 7440-56-4, uses and miscellaneous

RL: TEM (Technical or engineered material use); USES (Uses)
(IR absorber, for IR crystn. of polysilicon films for transistors)

RN 7440-56-4 HCAPLUS

CN Germanium (7CI, 8CI, 9CI) (CA INDEX NAME)

Ge

IT 7440-21-3, properties

RL: SPP (Properties); TEM (Technical or engineered material use); USES
(Uses)
(IR crystn. of polycryst., on germanium films)

RN 7440-21-3 HCAPLUS

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IT 7631-86-9, uses and miscellaneous

RL: USES (Uses)
(mask, for polysilicon crystn. in transistor fabrication)

RN 7631-86-9 HCAPLUS

CN Silica (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

O==Si==O

114 ANSWER 3 OF 4 HCAPLUS COPYRIGHT 2003 ACS on STN
 AN 1980:119708 HCAPLUS
 DN 92:119708
 TI Electrophotographic plates
 IN Komatsu, Toshiyuki; Hirai, Hiroshi; Nakagawa, Katsumi; Fukuda, Chuji
 PA Coton X. K., Japan
 SO Jpn. Kokai Tokkyo Koho, 20 pp.
 CODEN: JKXXAF
 DT Patent
 LA Japanese
 IC G03G005-08; G03G005-04
 CC 74-3 (Radiation Chemistry, Photochemistry, and Photographic Processes)
 PAF.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 54145541	A2	19791113	JP 1978-53607	19780504
JP 61061104	B4	19861224		
PRAI JP 1978-53607		19780504		

AB Electrophotog. plates comprising an amorphous Ge layer having homojunction type depletion layer as the photoconductor layer, and a transparent surface layer. The depletion layer acts as the charge carrier-generating layer. The electrophotog. plate may also have a barrier layer and also an elec. insulating top layer. The homojunction may be a p-n, i-p, or i-n junction. The electrophotog. plates exhibit excellent sensitivity, and give copies with high resoln., high optical d., and good halftone reproducibility. Thus, amorphous Ge is deposited on a glass support having a transparent In2O3 conductor layer by using chem. vapor deposition from GeH₄, then B-doped Ge is deposited from a GeH₄-B2H₆ mixt., and the Ge layer is overcoated with a polycarbonate resin to give an electrophotog. plate. The electrophotog. plate gave copies with high resoln. and good halftone reproducibility.

L121 ANSWER 7 OF 8 HCAPLUS COPYRIGHT 2003 ACS ON STN

AN 1994:546817 HCAPLUS

DN 121 146817

TI Manufacture of semiconductor device with low strain

IN Tanho, Toshiharu

PA Matsushita Electronics Corp, Japan

SO JPN Kokai Tokkyo Koho, 4 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

IC ICM: H01L021-338

ICS: H01L029-812; H01L021-28

CC 76-3 (Electric Phenomena)

FAN CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
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PI JP 06069243 A2 19940311 JP 1992-221075 19920820

PRAI JP 1992-221075

AB The titled device is manufactured by a process including following successive steps: (1) forming the 1st conductive semiconductor layer on a main face of a substrate, (2) forming a gate electrode on the 1st conductor, (3) removing the surface of the 1st semiconductor by using the gate electrode as a mask, (4) forming high-concn. the 2nd semiconductor layer of the same cond. to the 1st by self alignment, (5) heating the substrate, (6) forming an elec. insulator film on a main face of the substrate, and (7) forming an ohmic electrode on the 2nd semiconductor layer. The resulted device shows small fluctuation of mutual conductance in the driving region.

IT Transistors

(field-effect insulated-gate, with low strain,
manuf. including self alignment of ohmic electrode for)

IT 7440-56-4. Germanium, uses

RL: USES (Uses)
(ohmic electrode including, self-aligned bottom layer for,
for low strain thin film transistor)

RN 7440-56-4 HCAPLUS

CN Germanium (7C1, 8C1, 9C1) (CA INDEX NAME)

Ge

L123 ANSWER 11 OF 21 HCPLUS COPYRIGHT 2003 ACS on STN
 AN 1995:923801 HCPLUS
 DN 124:16104
 TI B incorporation in Ge(001) grown by gas-source molecular-beam epitaxy from
 Ge2H6 and B2H6
 AU Liu, O.; Brumblatt, T. R.; Hasan, M.-A.; Lee, N.-E.; Greene, J. E.
 CS Materials Res. Lab., Univ. Illinois, Urbana, IL, 61801, USA
 SO Journal of Applied Physics (1995), 78(10), 6027-32
 CODEN: JAPIAU; ISSN: 0021-8979
 PB American Institute of Physics
 DT Journal
 LA English
 CC 66-3 (Surface Chemistry and Colloids)
 Section cross-reference(s): 75, 76
 AB SIMS was used to det. the concn. and depth distribution of B incorporated
 into Ge (001)2.times.1 films grown on Ge (001)
 substrates by gas-source MBE using Ge2H6 and B2H6. The B concns. (CB = 3
 .times. 10¹⁶-10¹⁷ cm⁻³) increase linearly with
 increasing flux ratio (B2H6/Ge2H6 = 1.0-10⁻³-1.7) at const. film
 growth temp. (T_G = 300-400.degree..) and increase exponentially with 1/T_G
 at const. B2H6/Ge2H6 ratio. The difference in the overall activation
 energies for B and Ge incorporation over this growth
 temp. range is 0.22 eV while B2H6 reactive sticking probabilities range
 from 8 times. 10⁻⁴ at 300.degree.. to 2 times. 10⁻⁵ at 400.degree.. SIMS
 depth profiles from n modulation-doped samples and
 2-dimensional delta-doped samples grown at T_G < 350.degree.. were abrupt
 to within instrumental resoln. with no indication of surface segregation.
 Structural anal. by in situ RHEED combined with postdeposition
 high-resoln. plan-view and cross-sectional TEM showed that all films were
 high-quality single crystals with no evidence of dislocations or other
 extended defects. The B doping had no measurable
 effect on Ge deposition rates.
 IT 7440-56-4, Germanium, properties
 RL PRP (Physical, engineering or chemical process); PRP (Properties); TEM
 (Technical or engineered material use); PROC (Process); USES (Uses)
 (SIMS depth profile study of B incorporation in Ge (001) grown by
 gas-source MBE from B2H6 and Ge2H6)

123 ANSWER 7 OF 21 HCAPLUS COPYRIGHT 2003 ACS on STN

AN 50011630924 HCAPLUS

DW 135188773

TI Gate stack structure for variable threshold voltage

IN Yu, Bin; Adem, Ercan

PA Advanced Micro Devices, Inc., USA

SO U.S., 25 pp.

CODEN: USXXAM

DT Patent

LA English

IC ICM HO1L031-119

NCL 257407000

CC 76-3 (Electric Phenomena)

FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6281559	Bl	20010828	US 1999-261274	19990303

PRAI US 1999-261274

AB 19990303

An ultra-large-scale integrated (ULSI) circuit includes MOSFETs which have different threshold voltages and yet have the same channel characteristics. The MOSFETs include gate structures or gate stacks with a Si and Ge material provided over a seed layer. The seed layer can be a 20-40 \AA polysilicon layer. An amorphous Si layer is provided over the Si and Ge material, and a cap layer is provided over the amorphous Si layer. The polysilicon material is implanted with lower concns. of Ge, where lower threshold voltage MOSFETs are required. Over a range of 0-60 concn. of Ge, the threshold voltage can be varied by roughly 240 mV.

RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
 (CVD; silicon germanium compd. semiconductor gate stack structure for variable threshold voltage in ULSI circuits)

IT 7440-45-8, Boron uses

RL: MOA (Modifier or additive use); USES (Uses)
 (ion implanting; silicon germanium compd.
 semiconductor gate stack structure for variable threshold voltage in ULSI circuits)

IT 7440-56-4, Germanium processes

RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
 (silicon germanium compd. semiconductor gate stack
 structure for variable threshold voltage in ULSI circuits)

L114 ANSWER 4 OF 4 HCPLUS COPYRIGHT 2003 ACS on STN
 AN 1970:94467 HCPLUS
 DN 72:94467
 TI Anomalous thermal behavior of boron-doped low-temperature germanium
 epitaxial layers
 AU Bekeznalit, A.; Light, T. B.; Reisman, A.
 CS Watson Res. Center, IBM, Yorktown Heights, NY, USA
 SO Journal of the Electrochemical Society (1970), 117(3), 359-62
 CODEN: JESOAN; ISSN: 0013-4651
 DT Journal
 LA English
 CC 71 (Electric Phenomena)
 AB Recently, conditions have been defined for the growth of mirror-smooth
 layers of Ge on either Ge or semi-insulating Ga-As by the Ge-
 disproportionation reaction. In attempting to dope these layers with
 p-type impurities under the defined surface-rate-limited growth
 conditions, order-of-magnitude decreases in resistivity occurred on
 heating the grown layer to temperatures above the original growth temp.
 This indicated that impurities were initially incorporated in an elec.
 inactive state. Results are presented which show this behavior to be
 increasingly pronounced for fast growth rates and low substrate temps.,
 and growth conditions to minimize the effect are defined.
 ST boron doped Ge; germanium B doped; exitaxial
 Ge layers

L103 ANSWER 22 OF 24 HCAPLUS COPYRIGHT 2003 ACS on STN

AN 1984:464472 HCAPLUS

DN 101:64472

TI Thin-film transistors

IN Nakagiri, Takashi; Hirai, Yutaka; Osada, Yoshiyuki

PA Canon K. K., Japan

SO Ger. offen, 46 pp.

CODEN: GWXXBX

DT Patent

LA German

IC H01L029-04; H01L029-78; H01L031-02; G09F009-35; G02F001-015

CC 76-3 (Electric Phenomena)

FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
DE 3331601	A1	19840308	DE 1983-3331601	19830901
DE 3331601	C2	19870430		
JP 59124175	A2	19840310	JP 1982-152105	19820902
JP 59124163	A2	19840718	JP 1982-231521	19821229
US 4740829	A	19880426	US 1986-937432	19861203

PRAI JP 1982-153105 19820902

JP 1982-231521 19821229

US 1983-527385 19830829

AB A stable and highly conductive thin-film transistor is fabricated with a polycryst. Ge or Ge-Si film contg. 1toreq. 3 at.% H. Thus, a Corning Glass no. 7059 washed with an HF-HNO₃-HOAc soln., there was coated 1st a Ge-0.3 at.% H film at 400.degree. from a glow discharge in a gas mixt. of GeH₄-H₂-B₂H₆, a similar Ge film from a GeH₄-H₂-PH₃ mixt., a SiNH film from a SiH₄-H₂-NH₃ mixt., and after pattern etching, with Al contacts to form an FET.

IT Transistors

(field-effect, thin-film, fabrication of with polycryst.
germanium and silicon films contg. hydrogen)

L121 ANSWER 6 OF 8 HCAPLUS COPYRIGHT 2003 ACS on STN

AN 1998:545517 HCAPLUS

DN 129:238626

TI Semiconductor device.

IN Yamazaki, Shunpei

PA Semiconductor Energy Laboratory Co., Ltd. (SEL), Japan

SO Jpn. Kokai Tokkyo Koho, 10 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

IC ICM H01L029-786

ICS H01L029-78

CC 76-3 (Electric Phenomena)

FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
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PI JP 10223909 A2 19980921 JP 1997-40089 19970208

PRAI JP 1997-40089 19970208

AB A semiconductor device such as a TFT comprises a gate electrode such as Al, polycrystalline silicon, or W silicide formed on a **gate insulator film**, or W silicide formed on a **gate insulator film** via material such as W, Ti, or Ge having a work function different from that of the gate electrode to control its threshold values

IT 7440-21-3, Silicon, uses

RL: DEV (Device component use); USES (Uses)
(polycryst.; gate electrode of semiconductor device)

IT 7440-56-4, Germanium, uses

RL: DEV (Device component use); USES (Uses)
(gate electrode of semiconductor device)

RN 7440-56-4 HCAPLUS

CN Germanium (7CI, 8CI, 9CI) (CA INDEX NAME)

Ge

L123 ANSWER 17 OF 21 HCPLUS COPYRIGHT 2003 ACS on STN
 AN 1989:86367 HCPLUS
 DN 110:86367
 TI Epitaxial growth and band bending of n- and p-type
 germanium gallium arsenide (001)
 AU Chambers, S. A.; Irwin, T. J.
 CS Mater. Dev. Lab., Boeing Electron. High Technol. Cent., Seattle, WA,
 98124-6269, USA
 SO Physical Review B: Condensed Matter and Materials Physics (1988), 38(11),
 7484-92
 CODEN: PRBMDO; ISSN: 0163-1829
 DT Journal
 LA English
 CC 76-2 (Electric Phenomena)
 Section cross-reference(s): 66, 73
 AB High-resoln. XPS, LEED, and x-ray photoelectron diffraction were combined
 to examine the interface structure and band-bending characteristics of n-
 and p-type Ge epilayers grown on semiconducting
 insulating GaAs(001). The 1st monolayer of Ge intermixes with
 atoms at the clean surface, resulting to yield a complex structure. Subsequent
 Ge monolayers grow epitaxially but exhibit surface roughness in the form
 of local variation in layer thickness of the order of 2-3 monolayers (3-4
 Ång.), in agreement with previous RHEED measurements obtained during
 continuous overlayer growth. The growth of undoped (which is actually
 p type) and As-doped Ge
 overlayers results in Schottky-barrier-height changes of +0.05 and
 -0.35 eV, resp., relative to the clean-surface value of 0.83 +/- 0.05 eV.
 The barrier height correlates directly with dopant level in the Ge
 epilayer. In contrast, the valence band offset is independent of dopant
 level in the Ge film and maintains a const. value of
 0.60 +/- 0.05 eV. With the exception of the barrier height of the
 starting surface, these results are the same as those obtained on n-type
 substrates, further supporting the conclusion that barrier-height
 formation and band-offset development occur independently.

L42 ANSWER 23 OF 29 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
 AN 1992-131697 [16] WPIX
 CR 1993-328086 [41]
 DNN NL1992-098226 DNC C1992-061652
 TI Germanium silicon di oxide gate MOSFET - comprises
 doped silicon substrate with silica gate and thin film of poly- silicon on
 gate oxide.
 AW METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR.
 DC L03 U11 U12
 IN OZTURK, M; WORTMAN, J
 PA (UNNC-N NORTH CAROLINA S UN
 CYC 1
 PI US 5101247 A 19920331 (199216)* 6p
 ADT US 5101247 A US 1990-515595 19900427
 PPAI US 1990-515595 19900427
 IC H01L029-10
 AB US 5101247 A UPAB 19931130
 A MOSFET, with a silica/poly-Si/Ge gate, formable at
 high throughput using little heat and using self-alignment, comprises a
 doped Si substrate (21) on which is a silica gate (22) with oppositely
 doped adjacent to source (23) and drain (24) forming pn junctions with the
 gate, and a thin film of poly-Si (25) on the gate oxide. This is thick
 enough to support a thin film Ge gate contact (26)
 which is then deposited upon it.
 Pref. the poly-Si film is only 10 (or 5) nm thick and pref. the Si
 substrate is a wafer comprising locally oxidised Si to isolate the
 transistor. Pref. there is an insulating passivating layer on source,
 drain and gate having openings for contacts. Pref. the Ge
 film is polycrystalline.
 USE/ADVANTAGE - A MOSFET having a silica/poly-Si/Ge
 gate structure (claimed) is provided which may be mfd. at high
 throughput with a lower thermal budget. The high temps. and low rates in
 poly-Si deposition are less of an obstacle since only a thin layer is
 needed to support the Ge, which is deposited at 350 deg.C by LPCVD.
 32/2
 Dwg.32/2
 FS CPI EPI
 FA AB; GI